UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,222	02/11/2004	Hirofumi Komori	1259-0243P	9988

2292 7590 12/29/2005

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
KRAIG, WILLIAM F	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/775,222	KOMORI, HIROFUMI
	Examiner	Art Unit
	William Kraig	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *10-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *3,8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *21104*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1-9 in the reply filed on 12/7/2005 is acknowledged. Applicant argues that withdrawn process claims which happen to depend from or otherwise include all the limitations of allowable product claims could be rejoined. This is not found persuasive because it is merely a statement of United States Patent and Trademark Office restriction and rejoinder policy found in M.P.E.P section 821.04.

The requirement is still deemed proper and is therefore made FINAL.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. The disclosure is objected to because of the following informalities: In the paragraph beginning on Line 12 of Page 2 of the specification, the word "burrier" should be replaced with --barrier-- on Lines 18, 21, and 23.

Appropriate correction is required.

Claim Objections

4. Claim 3 objected to because of the following informalities: As best understood, Examiner believes that claim 3 should depend from claim 2 and not from claim 1.

Claim 3 objected to because of the following informalities: There is an error on line 10 of the claim. The Examiner recommends the replacement of the word "is" with the word --are--.

Claim 8 objected to because of the following informalities: There is an error on line 12 of the claim. The Examiner recommends the replacement of the word "is" with the word --are--.

Claim 9 objected to because of the following informalities: There is an error on line 2 of the claim. The Examiner recommends the replacement of the word "being" with the word --is--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-9 rejected under 35 U.S.C. 103(a) as being unpatentable over Isogai et al. (U.S. Patent # 6188093) in view of Miida(U.S. Patent # 6476371).

Regarding claim 1, Figs. 1-4 of Isogai et al. disclose a solid-state imaging device equipped with plural unit pixels (Col. 25, Lines 12-15) each of which includes a photo-diode (1) and a photo-detector (2) on a substrate (100), the photo-diode (1) comprising a charge generating region (13) to generate charges upon light irradiation (Col. 20, Lines 42-43).

Isogai et al., however, fails to disclose the photo-detector comprising a charge accumulation region to accumulate the charges transferred from the charge generating region and generating a signal potential that changes in accordance with the amount of the charges in the charge accumulation region.

Fig. 2A of Miida teaches a photo-detector (112) comprising a charge accumulation region (25) to accumulate the charges transferred from the charge generating region and generating a signal potential that changes in accordance with the amount of the charges in the charge accumulation region (Col. 7, Lines 18-24)

It would have been obvious to one of ordinary skill in the art to incorporate the charge accumulating region of Miida into the device of Isogai et al. The ordinary artisan would have been motivated to modify Isogai et al. in the above manner for the purpose of changing the threshold voltage of the photodetector's MOS transistor in order to use the change in threshold voltage to detect the optical signal (Miida, Col. 7, Lines 17-24).

Isogai et al. and Miida further disclose the solid-state imaging device comprising:

a charge transfer region (Isogai et al., Fig. 3 (region disposed beneath transfer gate (3))) provided between the charge generating region (Isogai et al., Fig. 3 (13)) and the charge accumulation region (Miida, Fig. 2A (25)) of the pixel,

the charge transfer region (Isogai et al., Fig. 3 (region disposed beneath transfer gate (3)))

The claims to the charge transfer region forming a first potential barrier to the charges in the charge generating region and the first potential barrier being removable according to the applied voltage to the photo-detector are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Isogai et al. and Miida meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claim 2, Figs. 1-4 of Isogai et al. and Miida disclose the solid-state imaging device according to claim 1, further comprising a first charge eliminating region (Isogai et al., Figs. 1-4 (4)) formed between the substrate (Isogai et al., Fig. 3 (100)) and the charge accumulating region (Isogai et al., Fig. 3 (2)).

The claim to the charges in the charge accumulating region being eliminated to the substrate via said first charge eliminating region when a certain voltage is applied to the photo-detector is a purely functional limitation. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Isogai et al. and Miida meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claim 3, Figs. 1-4 of Isogai et al. and Miida disclose the solid-state imaging device according to claim 2, further comprising:

a second charge eliminating region (Isogai et al., Figs. 1-4 (6a)) formed near the charge generating region (Isogai et al., Figs. 1-4 (13)); and

a region (Isogai et al., Figs. 1-4 (16)), provided between the charge generating region (Isogai et al., Figs. 1-4 (13)) and the second charge eliminating region (Isogai et al., Figs. 1-4 (6a)).

The claims to the region forming a second potential barrier to the charges in the charge accumulating region and the second potential barrier being lower than the first potential barrier such that the charges in the charge eliminating region are overflowed to a surface side, opposite to the substrate, via the second charge eliminating region are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Isogai et al. and Miida meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claim 4, Figs. 1-4 of Isogai et al. and Miida disclose the solid-state imaging device according to claim 3.

The claim to the second potential barrier being removable according to the applied voltage to the second charge eliminating region is a purely functional limitation. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Isogai et al. and Miida meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claim 5, Figs. 1-4 of Isogai et al. and Miida disclose the solid-state imaging device according to claim 1, wherein the charge generating region (Isogai et al., Fig. 3 (13)) has one conductive type (Isogai et al., Col. 20, Lines 38-42), same as the substrate (Isogai et al., Col. 20, Lines 31-32), and the photo-diode (Isogai et al., Fig. 3 (1)) comprises a first region with opposite conductive type (Isogai et al., Fig. 3 (12)) that contacts the charge generating region (Isogai et al., Fig. 3 (13)), and wherein the photo-detector is a field effect transistor (Isogai et al., Col. 20, Lines 15-20) (Miida, Col. 4, Lines 57-61) and comprises:

a channel region (Miida, Col. 6, Lines 36-37 and 61-63) formed on the surfaces of the charge accumulating region (Miida, Fig. 2A (25)) with one conductive type (Miida, Col. 7, Lines 4-6) and the charge transfer region with opposite conductive type (Isogai et al., Fig. 3 (region disposed beneath transfer gate (3)));

a gate electrode formed on a gate insulation layer that is formed on the channel region (Miida, Col. 6, Lines 59-61);

a source region (Miida, Fig. 2A (16)) having opposite conductive type (Miida, Col. 6, Line 54), the source region near the charge accumulating region (Miida, Fig. 2A (25)) being connected to the channel region (Miida, Col. 6, Lines 36-37 and 61-63); and

a drain region (Miida, Fig. 2A (17b)) with opposite conductive type (Miida, Col. 6, Line 48) that is apart from the source region by the channel region (see Fig. 2A).

The claim to the signal potential being generated in the source region is a purely functional limitation. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Isogai et al. and Miida meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claim 6, Figs. 1-4 of Isogai et al. and Miida disclose the solid-state imaging device according to claim 5, wherein the plural pixels are arranged in first (vertical) and second (horizontal) directions to form a matrix (Miida, Col. 7, Lines 45-48), the source regions of the pixels along the first direction being connected to one another (Miida, Col. 8, Lines 2-5), the gate electrodes of the pixel along the second direction being connected to one another (Miida, Col. 7, lines 58-60) and the drain regions of all pixels being common (Miida, Col. 7, Lines 61-63).

Regarding claim 7, Figs. 1-4 of Isogai et al. and Miida disclose the solid-state imaging device according to claim 6, further comprising:

a switch circuit capable of electrically connecting and disconnecting the source region and the drain region of the pixel (Miida, Col. 8, Lines 22-27 and 46-49); and

a first charge eliminating region (Isogai et al., Figs. 1-4 (6a)) formed between the substrate (Isogai et al., Fig. 3 (100)) and the charge accumulating region (Isogai et al., Fig. 3 (2)).

The claims to the charges in the charge accumulating region being eliminated to the substrate via the first charge eliminating region when the potentials of the charge accumulating region and the charge transfer region are increased by boosting up the voltage to the gate electrode and wherein the voltage to the gate electrode is boosted by applying a voltage to the source and drain regions simultaneously while keeping the gate electrode at a high impedance state are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Isogai et al. and Miida meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claim 8, Figs. 1-4 of Isogai et al. and Miida disclose the solid-state imaging device according to claim 6, further comprising:
a second charge eliminating region (Isogai et al., Figs. 1-4 (6a)) formed near the charge generating region (Isogai et al., Figs. 1-4 (13)), the second charge eliminating region (Isogai et al., Figs. 1-4 (6a)) having one conductive type; and
a second region with opposite conductive type (Isogai et al., Figs. 1-4 (16)), provided between the charge generating region (Isogai et al., Figs. 1-4 (13)) and the second charge eliminating region (Isogai et al., Figs. 1-4 (6a)).

The claims to the second region forming a second potential barrier to the charges in the charge accumulating region and the second potential barrier being lower than the first potential barrier such that the charges in the charge eliminating region are overflowed to a surface side opposite to the substrate, via the second charge

eliminating region are purely functional limitations. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Isogai et al. and Miida meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Regarding claim 9, Figs. 1-4 of Isogai et al. and Miida disclose the solid-state imaging device according to claim 8.

The claim to the second potential barrier being removable according to the applied voltage to the second charge eliminating region is a purely functional limitation. It is well known that similar structures have similar characteristics and functions. Thus, as the device of Isogai et al. and Miida meets the structural and methodological limitations of this claim, it should also be able to exhibit similar functional capabilities.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tredwell et al., Sin, McGrath, Nakashiba, Patrick, Mouli, Hong, and Sasaki (U.S. Patent and Publication #s 5859462, 6136629, 6169318, 6498622, 20040188727, 20050001246, 20050012168, and 6150676, respectively) all disclose similar semiconductor devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Kraig whose telephone number is 571-272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFK

GEORGE ECKERT
PRIMARY EXAMINER